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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,202	02/16/2004	Ying-Yao Lin	REAP0008USA	2201

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/708,202	LIN ET AL.
	Examiner	**Art Unit**
	Linh V. Nguyen	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,12-19,21,22,26,27* is/are rejected.

7)☒ Claim(s) *6,9-11,20 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/5/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 10/6/05. Claims 14 – 27 have been added. Claims 1 – 27 are pending on this application.

Examiner's Comment

2. Incorrect application No. on pages 2 – 9 of the **Amendment**.

Response to Arguments

3. Applicant's arguments filed 10/16/05 have been fully considered but they are not persuasive.

With respect to claim 1, under remark applicant' argued that voltage- gain Av = K/ 1+ $\exp^{(Vy/Vt)}$ of AAPA is not a simple exponential function. Examiner respectful disagrees from the following:

A v = K/ 1+ $\exp^{(Vy/Vt)}$ of AAPA (Fig. 2) teaches the voltage gain Av varies according to the exponential function of $\exp^{(Vy/Vt)}$. Therefore, the voltage gain Av of AAPA is an exponential function. Since the simple exponential function in the claim did not distinct from AAPA 's exponential function; therefore the exponential function of AAPA clearly teaches the simple exponential function of the claimed invention.

Per explained above, the same rejection from previous office action is applying to original claims 1 – 5, 7, 8, and 13 in this office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claim 1 – 5, 7, 8, 13 and 27 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 1, Fig. 1 and 2 of AAPA discloses a variable gain amplifier (Fig. 1), comprising: an amplifying stage (differential transistors of Vin input to the base) for generating an output voltage out (V out) according to an input voltage (Vin') and a variable gain stage (differential transistor of Vy input to the base) for adjusting a voltage gain of the amplifying stage (Fig. 2 (AV)) according to at least a controlling volt age (Vy) wherein the voltage gain is a simple exponential function (Fig. 2), and the value of the simple exponential function is determined by the controlling voltage (Vy).

Regarding claim 2, wherein the simple exponential function (AV) comprises a function which raises a base (exp) to the power of an addition operation (Vy/Vt) of a argument, without an addition operation or a operation with a constant being perform on the function (Fig. 2 discloses Av = K/exp(Vy/Vt) without any addition or subtraction operation. Since, control voltage Vy>> than Vt then the constant 1 of Av function becomes insignificant)

Regarding claim 3, wherein the at least one controlling voltage comprises a first controlling voltage (Vy+ and a second controlling voltage (Vy-), and the value

of the simple exponential function is determined by the difference between the first and the second controlling voltages (this is inherent characteristic of Fig. 1, Since the Vout' and Vout" gain of are dependent upon the differential of controlling voltage Vy. Therefore the gain value of exponential function Av must be determined by the differential of voltage control signal Vy+ -) .

Regarding claim 4, wherein the variable gain stage (transistors of Vy+/Vy-) is a transconductance amplifier for generating a gain current (Iin' – Iout', I out') according to the difference between the first and the second controlling voltages (Vy +, Vy-).

Regarding claim 5, wherein the variable gain stage comprises: a first transistor coupled to the first controlling voltage (Transistor of Vy+) a second transistor coupled to the second controlling voltage (transistor of Vy-) ; a first current source (Transistor of Vin') coupled to the emitter of the first and the second transistors for providing a first current (Iin'), and a second current source (Vcc is a source for generating a current Iout' and Iin'- Iout') for generating the gain current, wherein the value of the gain current (Iin' – Iout') is determined by the first current (Iin') and the difference between the first and the second controlling voltages (Vy+, Vy -)

Regarding claim 7, wherein the amplifying stage (Fig. 1) comprises: an input unit (Transistor of Vin') coupled to the input voltage for generating an input current according to the input voltage (Vin') a current transforming unit (Transistor of Vy-) for generating a second current (Iout') according to the gain current (Iin' – Iout') and a transresistance (R) amplifying unit for generating the output voltage (Vout'), wherein the value of the output voltage is determined by the input current (Iin') and the second current (Iout').

Regarding claim 8, wherein the input unit comprises an input transistor (transistor of Vin's input) coupled to the in-put voltage (Vin') for generating the input current (Iin') according to the input voltage (Vin').

Regarding claims 13 and 27, wherein the variable gain amplifier is the half-circuit of a differential amplifier (Fig. 1 as applied to claim 1 above disclosing Iin', Iout', Vy, Vin' and Vout' is a half of differential amplifier circuit of Fig. 1).

6. Claims 12, 14 – 19, 21, 22, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki U.S. Patent No. 5,162,678.

Regarding claim 14, Fig. 1 of Yamasaki discloses a variable amplifier comprising: an amplifier stage (Q1, Q2, Q5, Q6) for generating an output voltage (Vo, Vo*) according to an input voltage (Vi, Vi*) a variable gain stage (Q7, Q8) for adjusting a voltage gain (see equations 3, 5 and 6 on pages 3 and 4) of the amplifying stage according to at least a controlling voltage (Vc, Vc*); wherein the voltage gain changes linearly decibel in response to the controlling voltage (Fig. 2).

Regarding claim 15, wherein the voltage gain changes linearly in decibel (Fig. 2) with respect to a simple exponential function (see equations 3, 5, 6 on pages 3 and 4), and the value of the simple exponential function determined by the controlling voltage (see equations 3, 5, 6 on pages 3 and 4).

Regarding claim 16, wherein the simple exponential function comprises a function raises a base to the power of an argument (See equation 3, 5, 6), without addition operation or a subtraction with a constant being performed on the function

(Equation 6 discloses a voltage gain Vo/Vin is an exponential function without addition operation or a subtraction with a constant being performed on the function).

Regarding claim 17, wherein the at least one controlling voltage (Vc – Vc*) comprises a first controlling voltage (Vc) and a second controlling voltage (Vc*) and the voltage gain changes linear in decibel according to the difference between the first and the second controlling voltages (Fig. 2).

Regarding claim 18, wherein the variable gain stage is a transconductance amplifier (Q7, Q8) for generating a gain current (see equation 5) according to the difference between the first and the second controlling voltage (Vc, Vc*).

Regarding claim 19, wherein the variable gain stage comprises: a first transistor (Q7) couple to the first controlling voltage (Vc); a second transistor (Q8)coupled to the second controlling voltage (Vc*); a first current source (IT) coupled to the emitter of the first and the second transistor for providing a first current (IT), and a second current source (I1, I2) for generating the gain current value (equation 5) wherein, of the current is determined by the first current (IT) and the difference between the first and second controlling voltages (equation 5).

Regarding claim 21, wherein the amplifying stage comprises an input unit (Q1, Q2) couple to the input voltage (VI, VI*) for generating an input current (I1) according to the input voltage; a current transforming unit (Q8) for generating a second current (I2) according to the gain current (IT); and transresistance amplifying unit (Q5, Q6) for generating the output voltage (Vo, Vo*) wherein the value of the output current voltage (Vo, Vo*) is determined by the input current (I1) and the second current (I2).

Regarding claim 22, wherein the input unit comprises an input transistor (Q1) couple to the input voltage (VI) for generating the input current (I1) according to the input voltage.

Regarding claims 26, wherein the voltage gain is expressed as C1xexp (C2(V1-V2)) wherein both C1 and C2 are constant value, V1 is the first controlling voltage and V2 is the second controlling voltage (See equation 3, 5, 6).

Regarding claim 12, the claim incorporated the same subject matter as of claim 26 and rejected along the same rationale.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claim 14 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim13 of copending Application No. 10/709,198. Although the conflicting claims are not identical, they are not patentably distinct from each other because both invention is claiming for a common subject matter: variable gain amplifier comprising a voltage gain that changes linearly in decibel in response to a controlling voltage.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach or suggest the variable gain stage further comprises: a first resistor coupled between the collector of the first transistor and the second current source; and a second resistor coupled between the collector of the second transistor and the second current source.

7. Claim 9 – 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 9, Prior art does not teach or suggest the variable gain stage comprises: wherein the current transforming unit comprises: a third transistor, the collector of the third transistor being coupled to the base of the third transistor; a fourth transistor; a third current source coupled to the

emitter of the third and the fourth transistors for providing and a third current; a fourth current source for generating the second current; whereby the ratio between the third current is substantially equivalent to current and the first the ratio between the second current and the gain current.

8. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach or suggest the variable gain stage further comprises: a first resistor coupled between the collector of the first transistor and the second current source; and a second resistor coupled between the collector of the second transistor and the second current source.

9. Claim 23 - 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 23, Prior art does not teach or suggest the variable gain stage comprises: wherein the current transforming unit comprises: a third transistor, the collector of the third transistor being coupled to the base of the third transistor; a fourth transistor; a third current source coupled to the emitter of the third and the fourth transistors for providing and a third current; a fourth current source for generating the second current; whereby the ratio between the third current is substantially equivalent to current and the first the ratio between the second current and the gain current.

Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Conclusion

11. Applicant's original claims are rejected with the same ground from previous office action, and the amended/new claims necessitated the new ground(s) of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

11/28/05

Linh Van Nguyen

Art Unit 2819